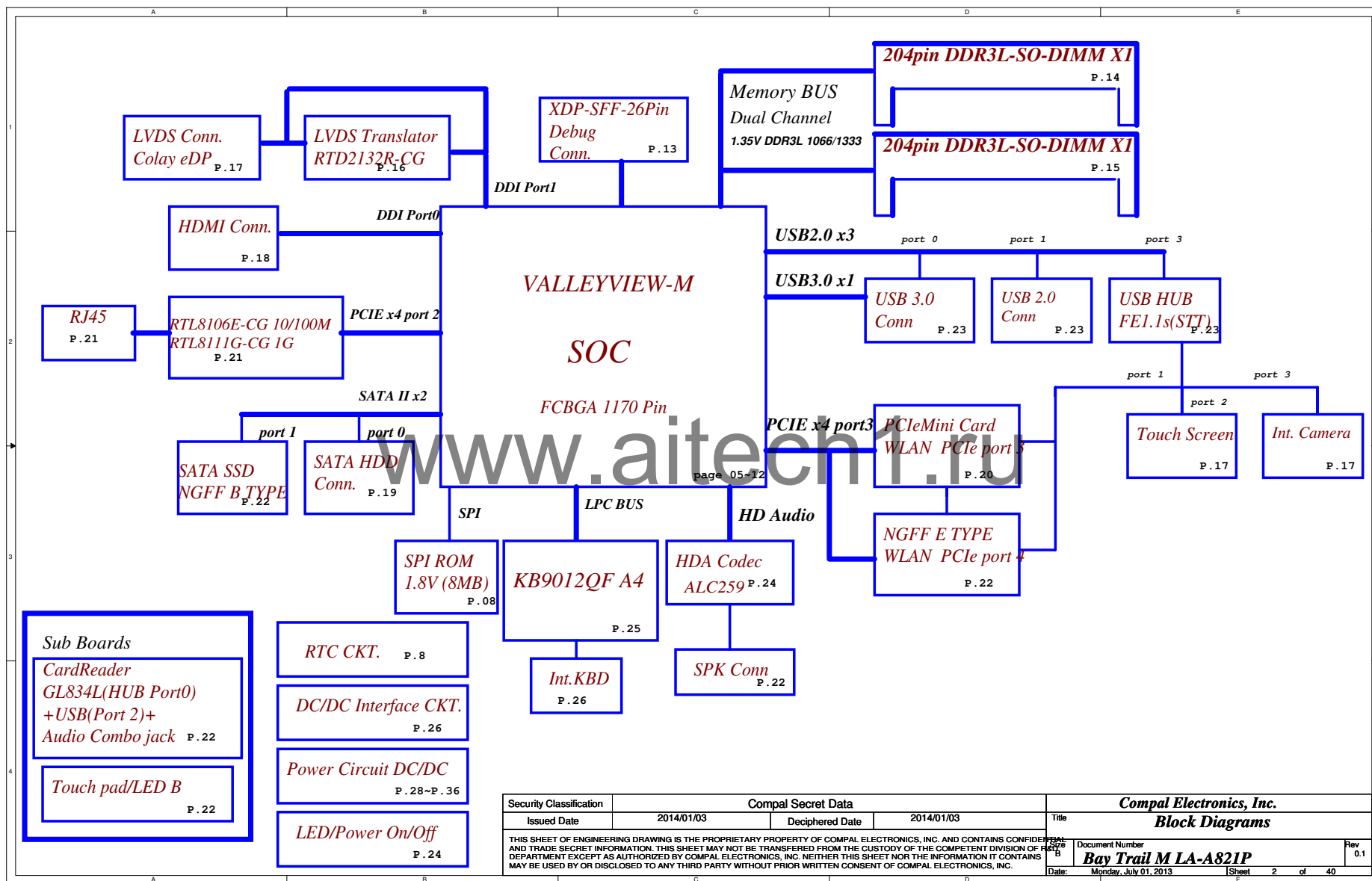


# Intel BayTrail-M Platform

Date : 2013/05/22  
Version 0.1

www.aitech1.ru

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/01/03	Deciphered Date	2014/01/03	Title	Cover Page
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				Bay Trail M LA-A821P	0.1
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## Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

## EC SM Bus2 address

Device	Address
--------	---------

## SOC SM Bus address

Device	Address
SO-DIMM A (JDIMM1)	A0h
SO-DIMM B (JDIMM2)	A2h

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	

## BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
XDP (Debug Port)	XDP@
EMC requirement	EMC@
EMC requirement unpop	@EMC@
TPM	TPM@
Touch Screen	TS@
R short	RS@
Test Point	TEST@

## BOM config

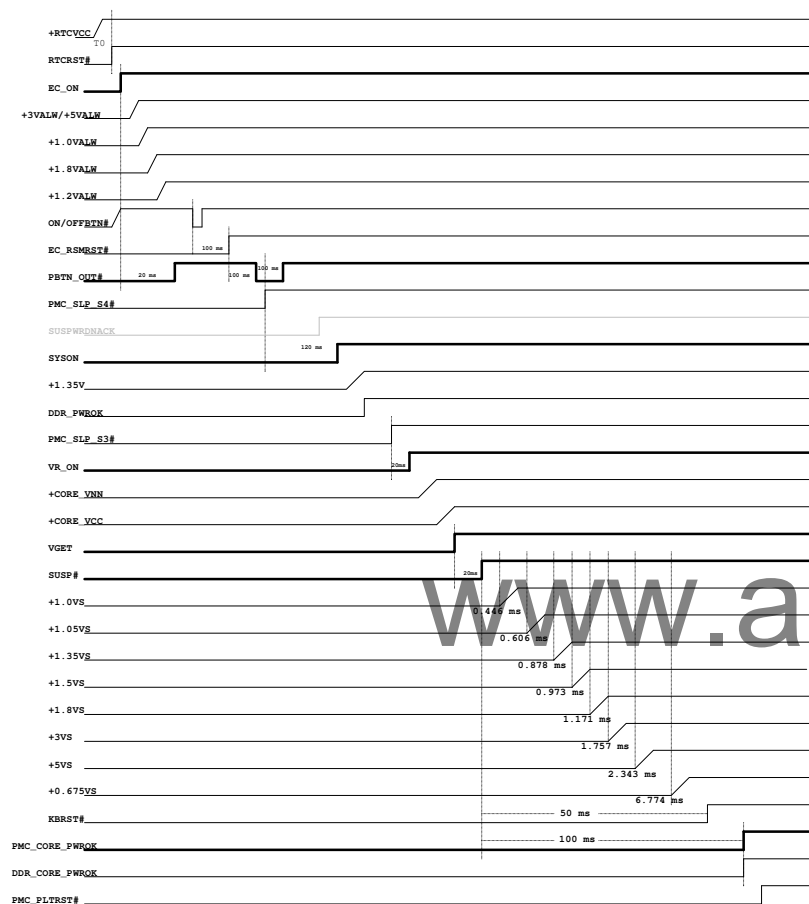
PCB P/N
EVT BOM config

## 43 level BOM table

43 Level	Description	BOM Structure
----------	-------------	---------------

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# Power ON

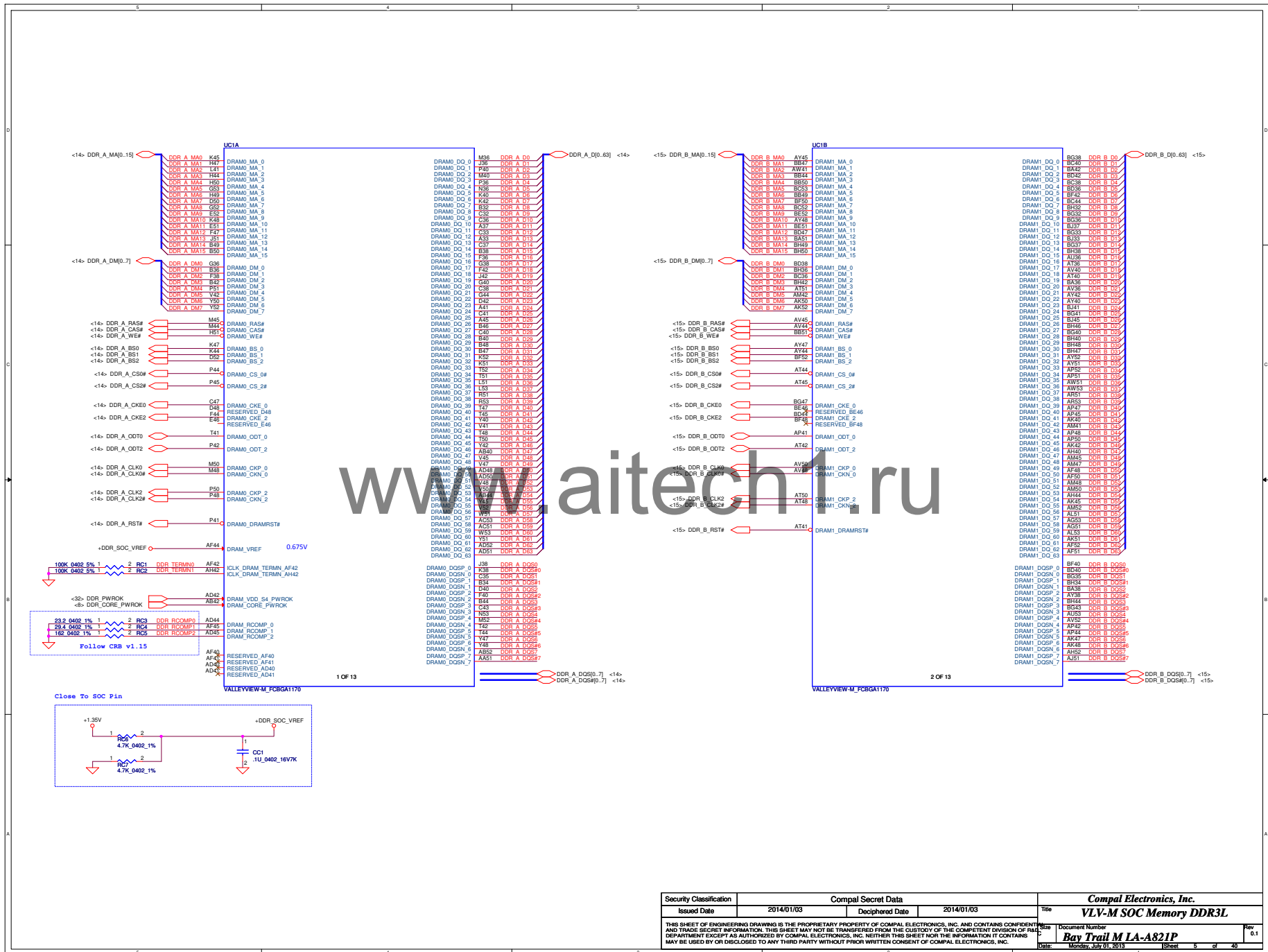


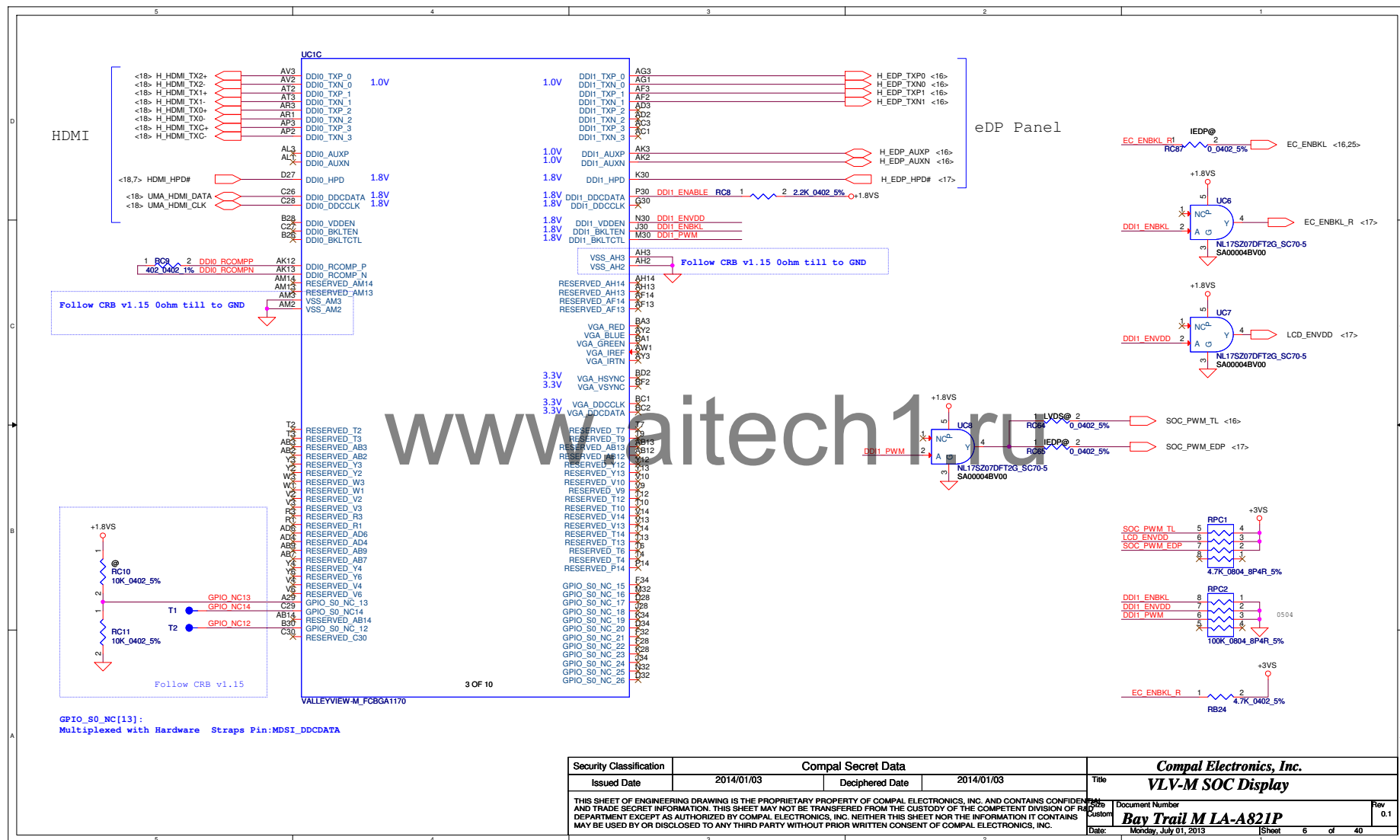
T0: +RTCVCC stable to RTCRST# high > 9ms  
T1: VR ramp up time from 10% to 90% voltage level < 2ms  
T2 :Rail to subsequent rail turn on delay < 2ms  
T3 :+VALWAS stable to EC\_RSMRST# high > 10ms  
T4 :+VS rails stable to PMC\_CORE\_PWROK > TBD

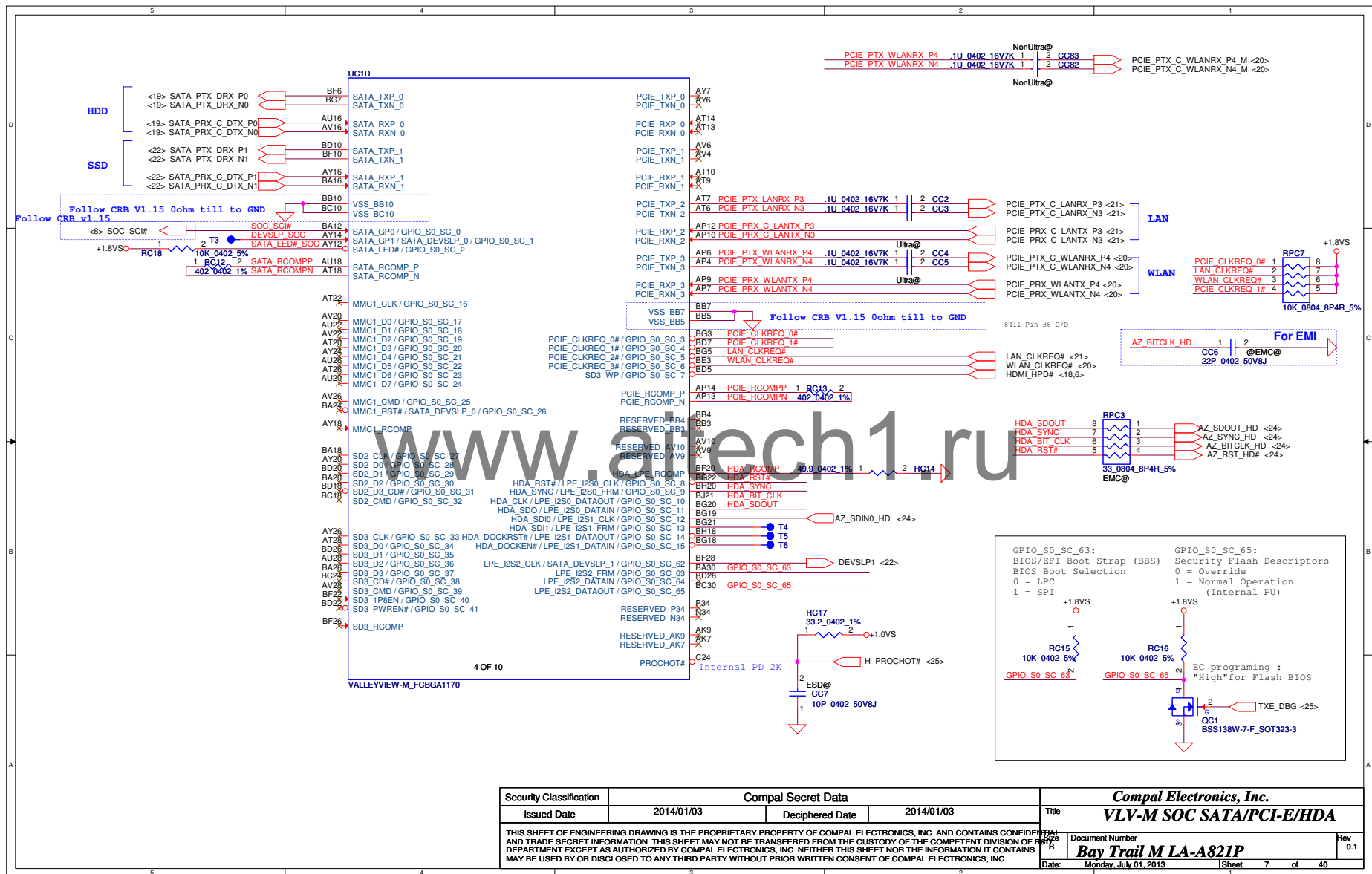
NOTE:  
1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.

2. Platform devices other than SOC sequencing are not explicitly shown as they are not limited by the SOC sequencing requirement.

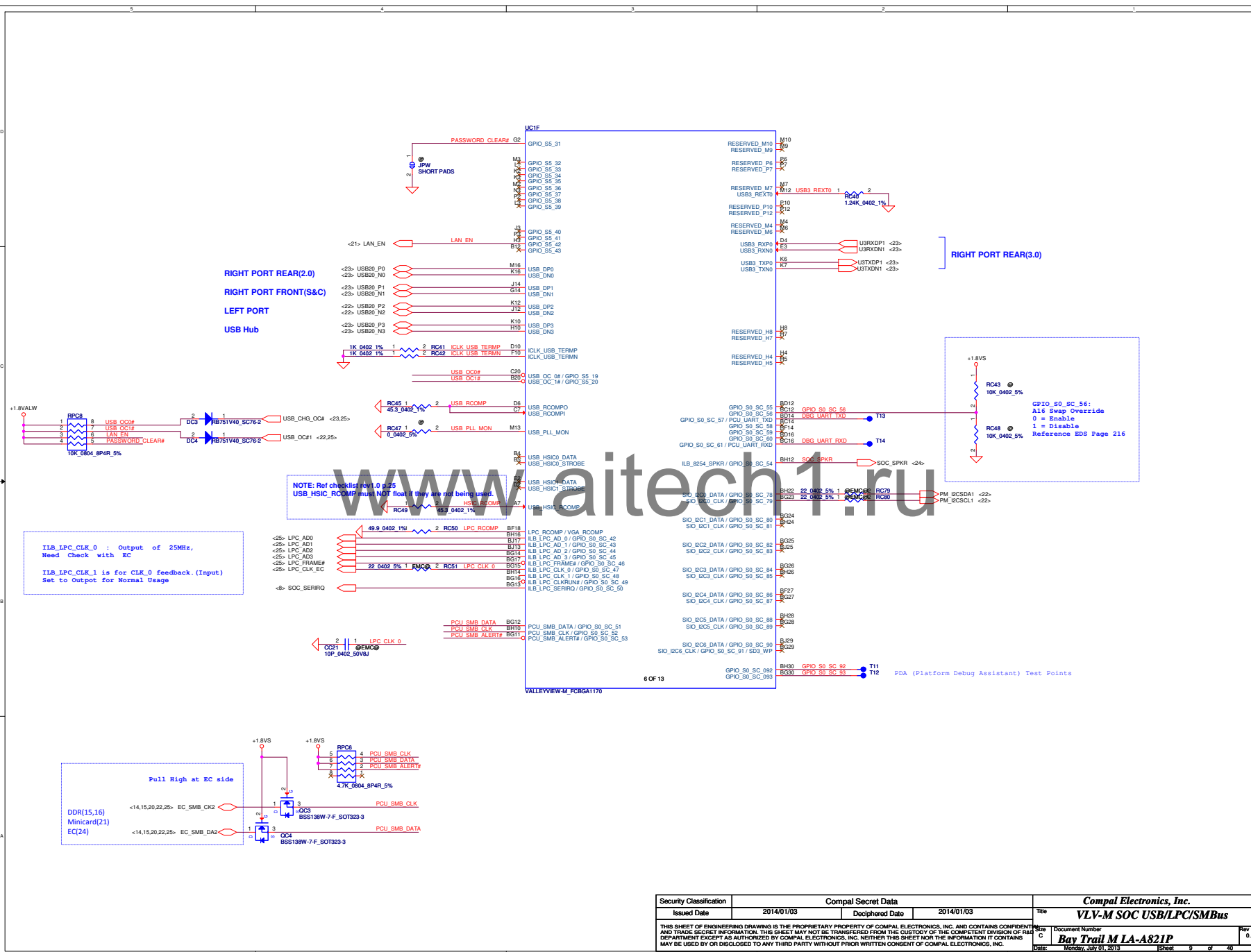
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/01/03	Deciphered Date	2014/01/03	Title
				Power Sequence
				Document Number
				Bay Trail M LA-A821P
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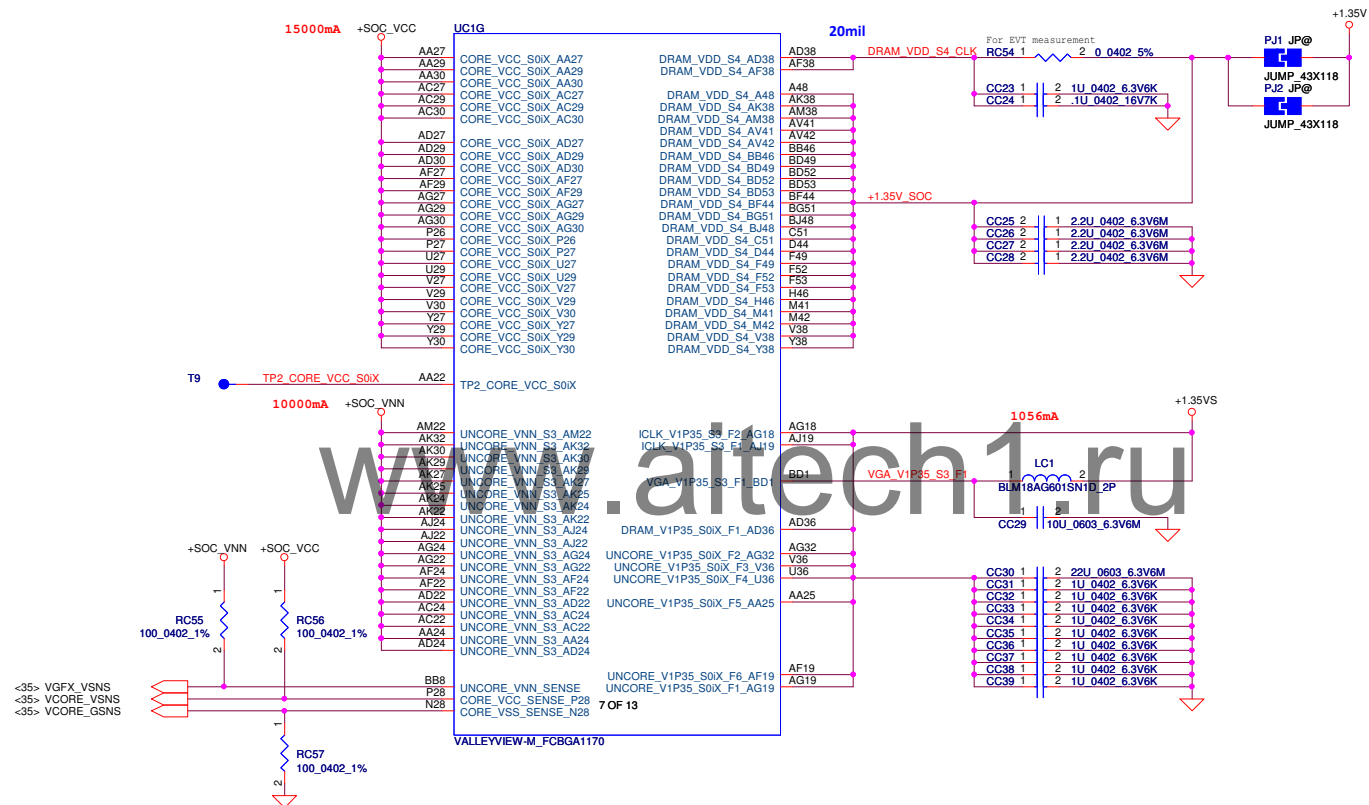




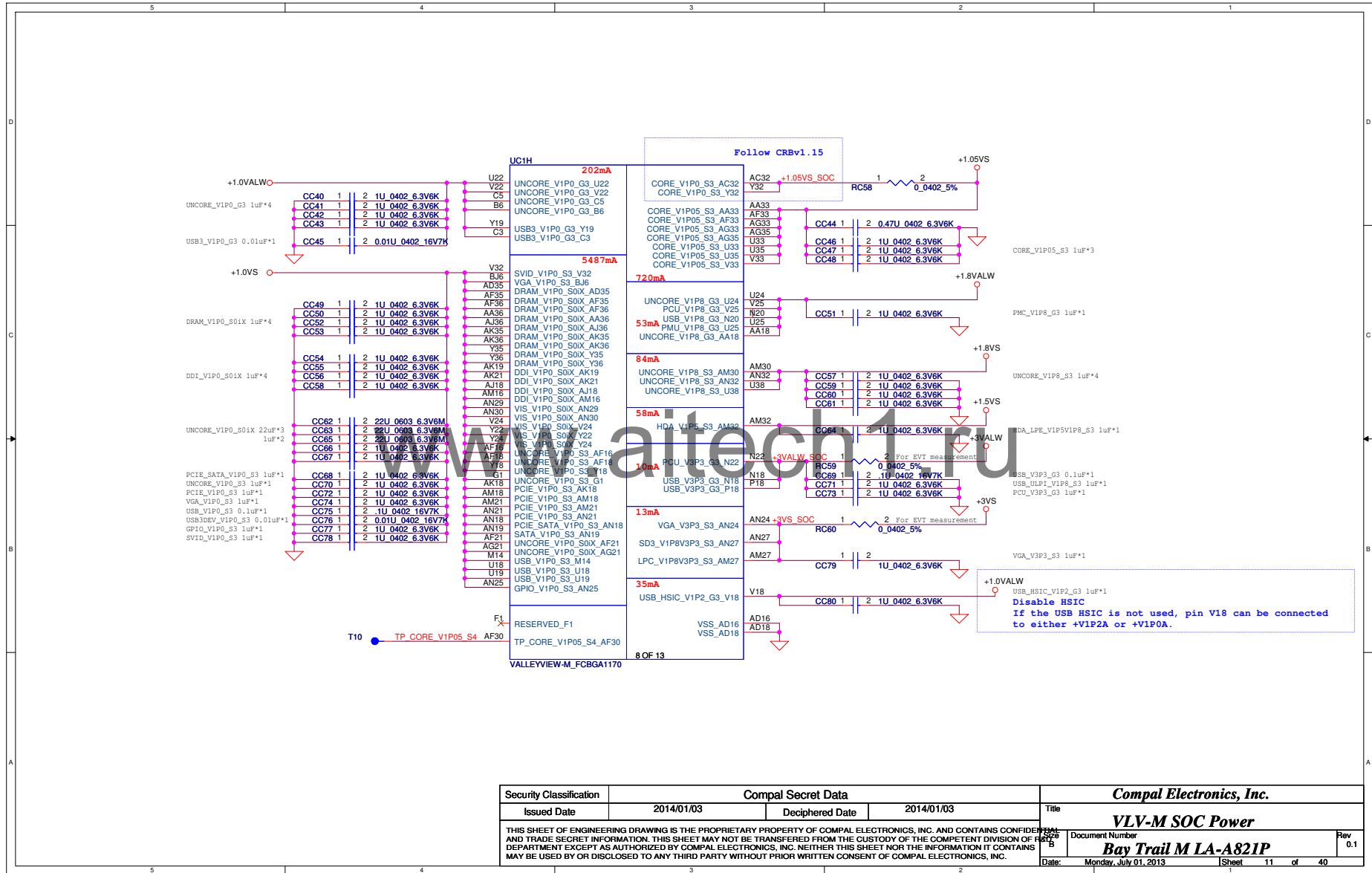


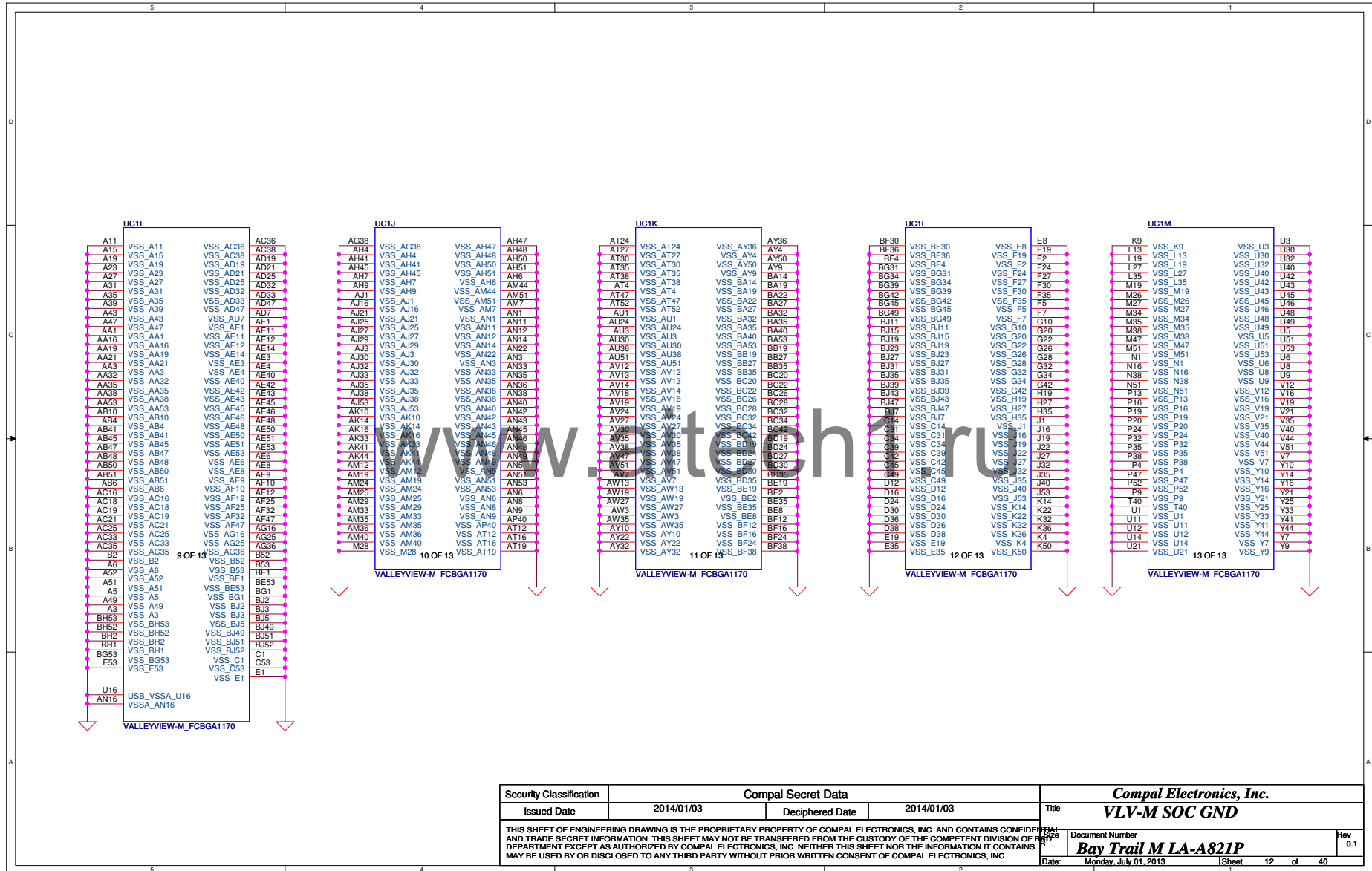


Security Classification	Compul Secret Data		Title		<b>Compul Electronics, Inc.</b>	
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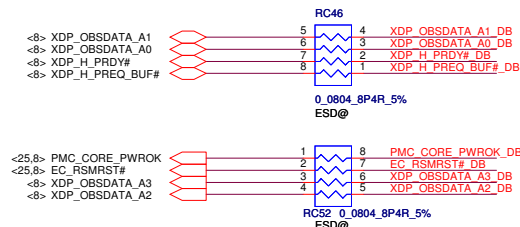
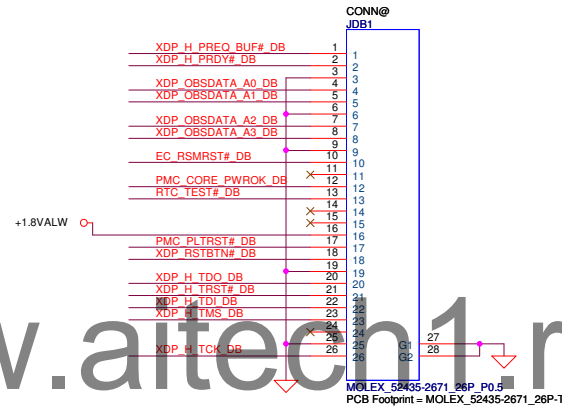


Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <b>VLV-M SOC Power</b>		
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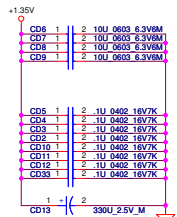


Timing diagram for MOLEX\_58435-2671\_26P\_P0.5. The diagram shows three signals: XDP\_H\_TDI\_DB, XDP\_H\_TMS\_DB, and XDP\_H\_TCK\_DB. The signals are plotted against time, with a large watermark 'www.aitech1.ru' overlaid. The signals show a sequence of logic levels (high and low) over time, with a large watermark 'www.aitech1.ru' overlaid.

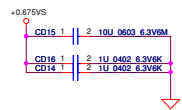


Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>VLV-M SOC Debug</b>	
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Layout Note:  
Place near JDIMM1

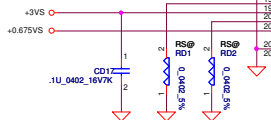


Part Number	Description	ESR
SF000002Z00	S_A-P_CAP 330U 2.5V M 6.3X4.2 R17M VLP5	17mΩ

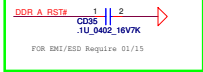


Layout Note:  
Place near JDIMM1.203,204

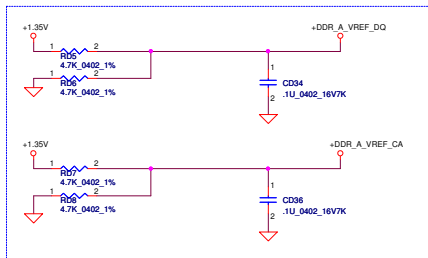
All VREF traces should  
have 10 mil trace width



<Address: SA1:SA0=00 (A0H)>  
**DIMM\_1 STD H:4mm**



Signal voltage level = 0.675 V  
PLACE TWO 4.7K RESISTORS CLOSE TO  
DIMM0 OR DIMM VREF\_CA / DIMM VREF\_DQ  
Decoupling caps are needed; one 0.1 µF placed close to VREF pins of each DDR3 SODIMM.

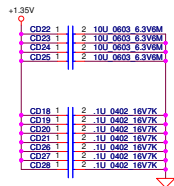


Part Number = SP07000JN10  
PCB Footprint = TYCO\_2013022-1\_204P

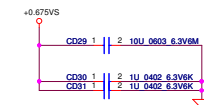
Channel A

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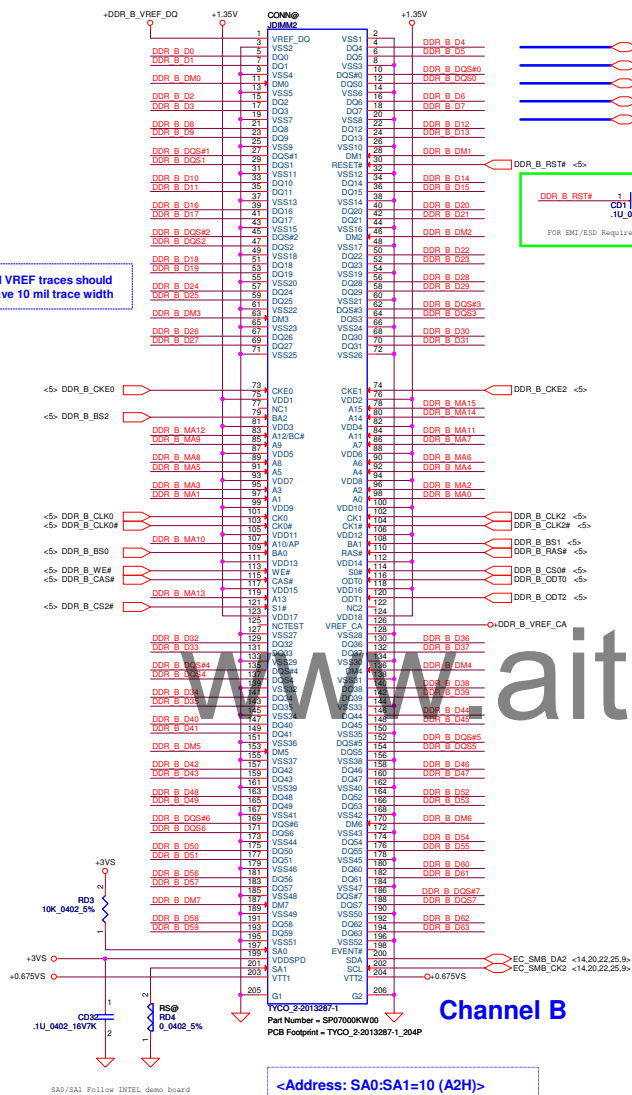
Layout Note:  
Place near JDIMM2



All VREF traces should  
have 10 mil trace width

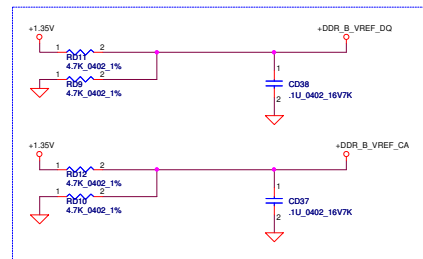


Layout Note:  
Place near JDIMM2.203,204

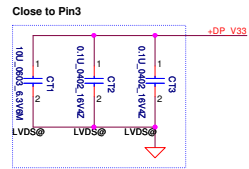
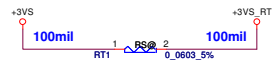


Channel B

<Address: SA0:SA1=10 (A2H)>  
DIMM\_2 REV H:4mm

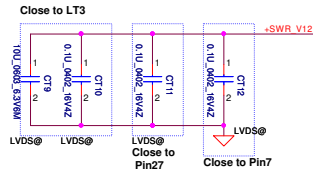
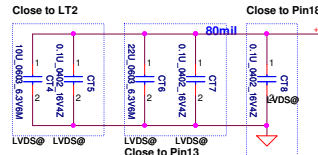


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### SWR / LDO Mode select

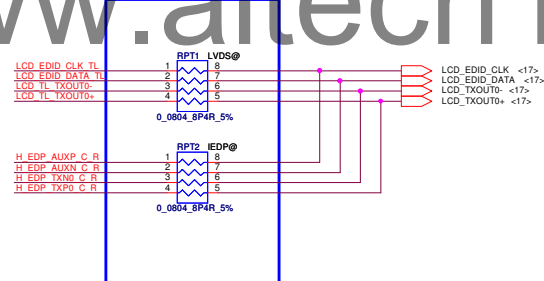
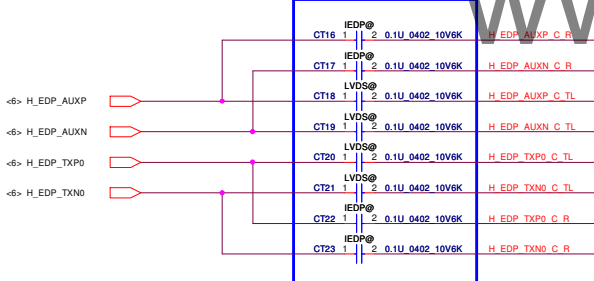
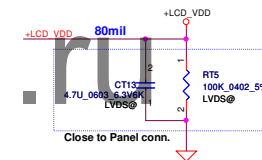
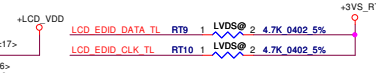
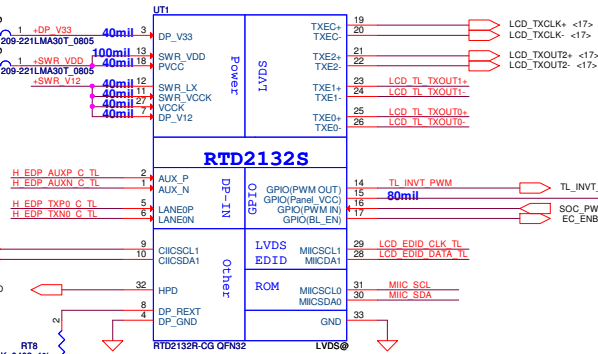
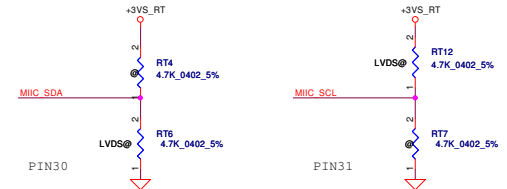
※LDO mode is adopted as default power regulator mode.  
Also can implement SWR mode by add inductor.



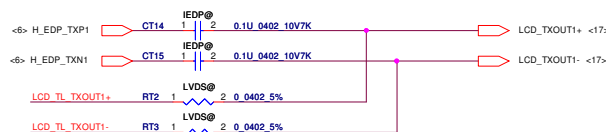
### Mode Configure

※ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.  
EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.  
EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.

< ※Default mode >



Place co-layer Resistor back to back on TOP and BOT



	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

\* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V
* Version R has internal level shifter, remove level shifter circuit on AMD platform	

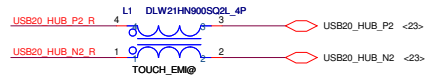
\* Version R has internal level shifter, remove level shifter circuit on AMD platform

### Different between 2132S and 2132R

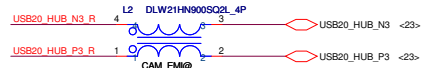
2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

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Size	Document Number	Rev	Bay Trail M LA-A821P	
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BTO : TOUCH\_EMI@

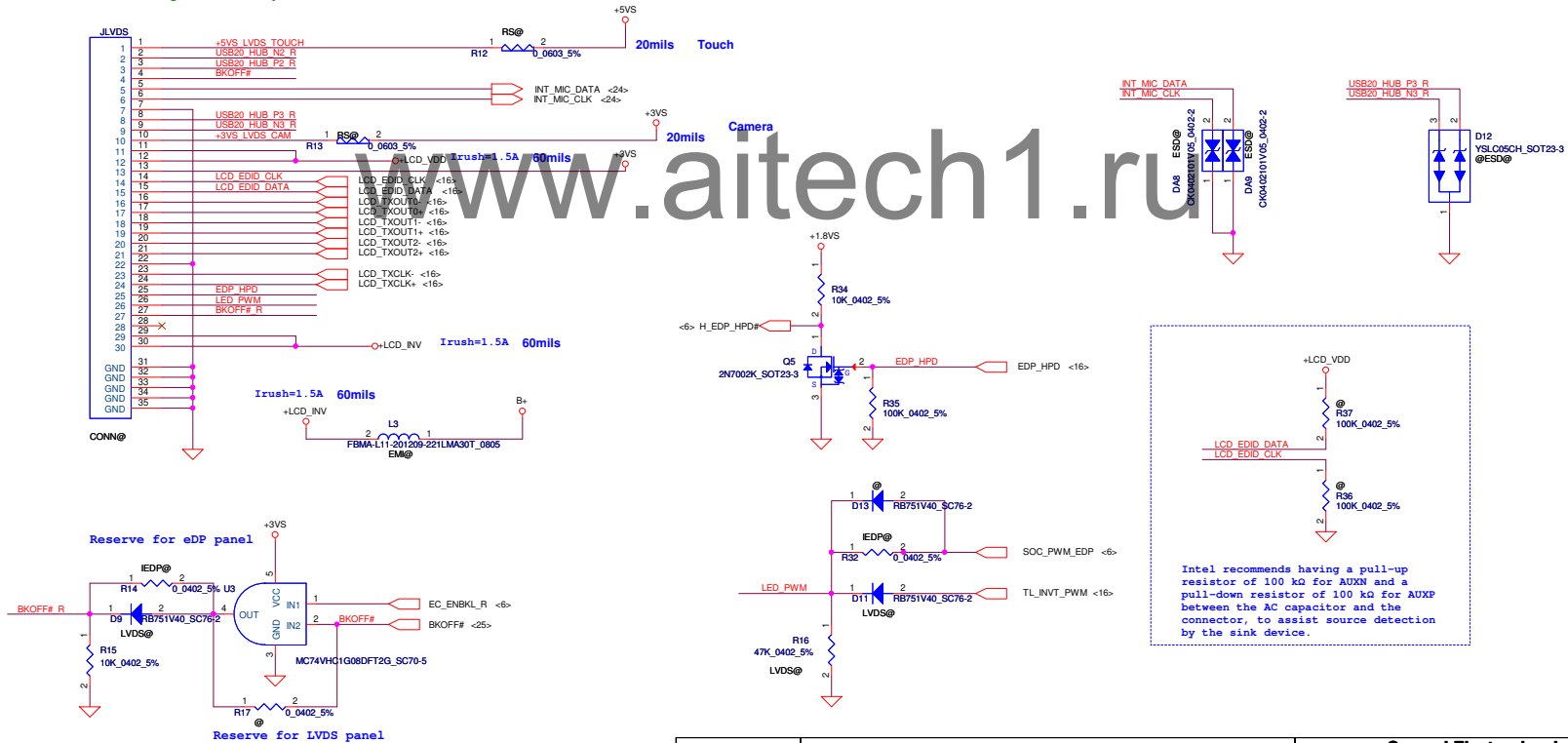


EMI request - Close to JEDP connector

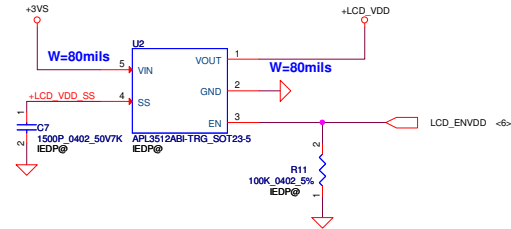


## LVDS colay eDP cable

Pin define will be change after ME ready



## LCD POWER CIRCUIT (For EDP panel only)



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HDMI Royalty

ZZZ1 HDMI45@

RO0000003HM

HDMI W/Logo + HDCP

HDMI W/O Logo: RO0000001HM

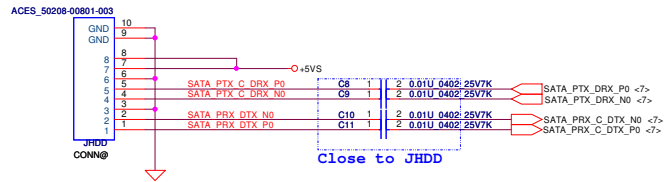
HDMI W/Logo: RO0000002HM

HDMI W/Logo + HDCP: RO0000003HM

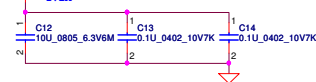
lease manually load  
his virtual material to 45@ BOM

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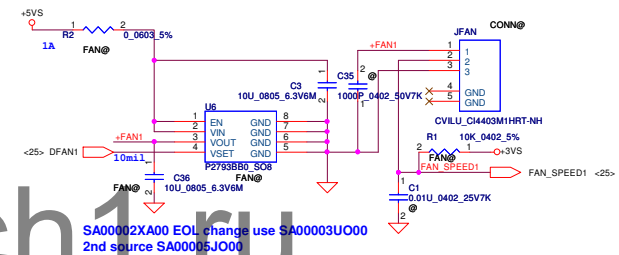
## SATA HDD Conn.



Place closely JHDD SATA CONN.



## FAN Control Circuit



www.aitech1.ru

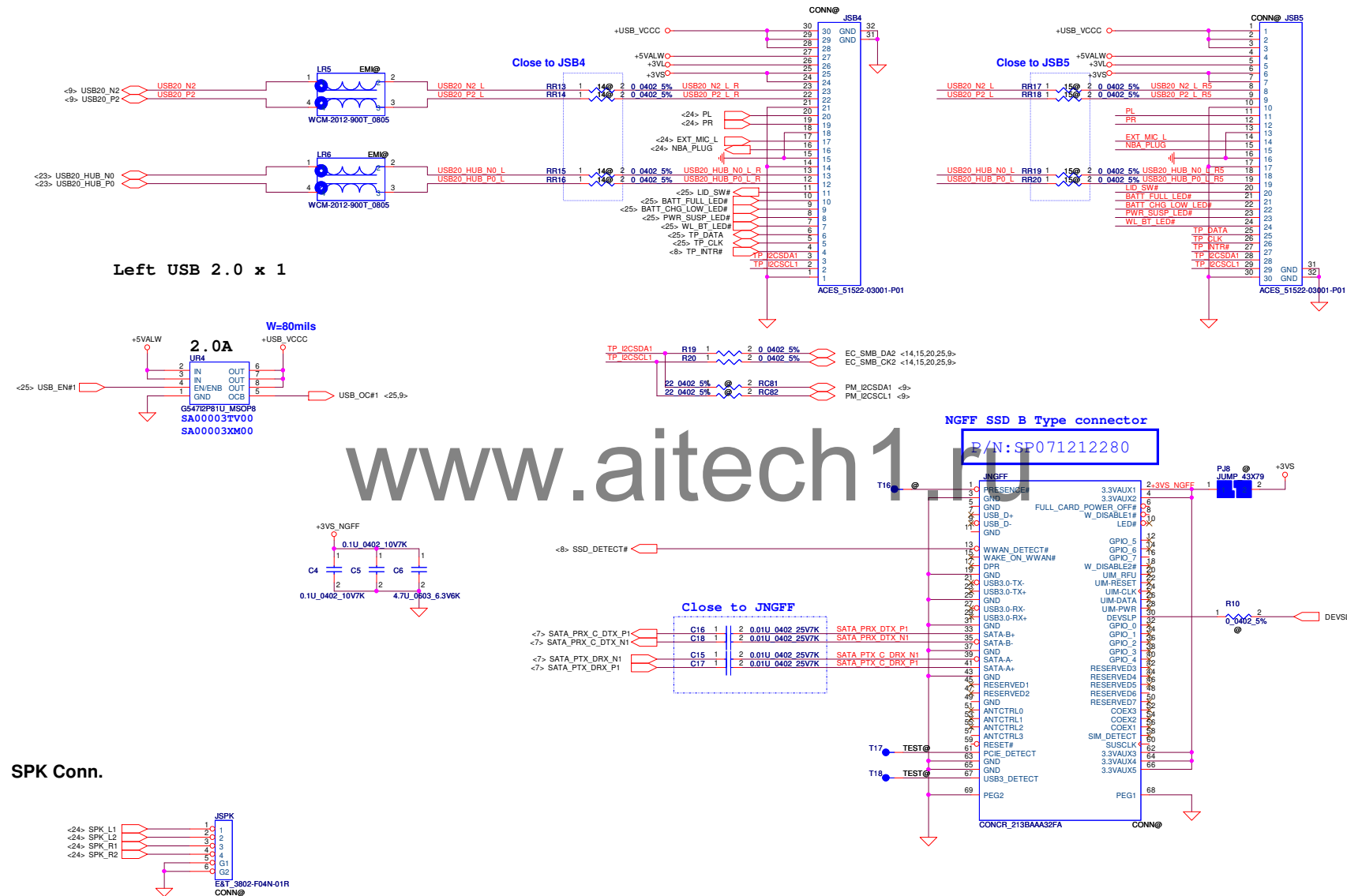
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[illegible][illegible]

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				Model	LA-A821P



## Small board Conn



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## USB Sleep & Charge

State table for TPS2546RTER

CB0	CB1	CB2	ILIM_SEL	Mode	STATUS
0	1	1	1	Auto	Auto-detection charger mode for Apple device(2A,1A). Resistor dividers are connected to DP/DM. Including DCP
1	0	1	1	Alternate	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	1	1	0	SDP	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	1	1	CDP	USB pass-through mode with CDP emulation. DP/DM are connected to TDP/TDM

CB0	CB1	CB2	ILIM_SEL	Mode	STATUS
0	1	1	1	Auto	Auto-detection charger mode for Apple device(2A,1A). Resistor dividers are connected to DP/DM. Including DCP
1	0	1	1	Alternate	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	1	1	0	SDP	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	1	1	CDP	USB pass-through mode with CDP emulation. DP/DM are connected to TDP/TDM

RIGHT REAR USB3.0 CONN.

Components and connections shown in the diagram:

- LR3 EMI@**: Inductor for USB20\_P0 and USB20\_N0.
- DLW21HN6005Q2L\_4P**: Component for USB20\_P0 and USB20\_N0.
- LR1 EMI@**: Inductor for U3RXDP1 and U3RXDN1.
- DLW21SN670H02L\_4P**: Component for U3RXDP1 and U3RXDN1.
- LR2 EMI@**: Inductor for U3TXDP1 and U3TXDN1.
- DLW21SN670H02L\_4P**: Component for U3TXDP1 and U3TXDN1.
- CR1, CR2**: Capacitors (0.1u 0402\_10V7K) for U3TXDP1 and U3TXDN1.
- 2.0A**: Current rating for the USB connection.
- W=80mils**: Width specification for the USB connection.
- USB\_VCCB**: USB VCCB connection.
- CR3, CR4, CR5**: Capacitors (0.1u 0402\_10V7K) for USB\_VCCB.
- 47U\_0805\_5.3V6M**: Capacitor for USB\_VCCB.
- 47U\_0603\_5.3V6M**: Capacitor for USB\_VCCB.
- DR1 @ESD@**: ESD protection diode for U3TXDN1 and U3RXDN1.
- TVWD1004AD0\_SL\_P2510P8-10-9**: Component for U3TXDN1 and U3RXDN1.
- JUSBR CONN@**: Connector for USB signals.
- SINGA\_2UB3914-000101F**: Component for USB signals.

**RIGHT FRONT USB 2.0 W/S&C**

UR3  
TPS244RTER\_QFN16\_3X3  
2544@

+5VALW

0.1u 0402 10V7K

W=100mils

2.5A

W=100mils

+USB\_VCCA

UR2  
TPS244RTER\_QFN16\_3X3  
2544@

Close to UR2 IN/OUT

+USB\_VCCA

W=100mils

CR13  
0.1u 0402 10V7K

CR12  
47u 0605 5.0V7K

CR15  
4.7u 0605 5.0V7K

RR11  
23.25 9%

RR12  
20K 0402 1%

RR10  
20K 0402 1%

USB20\_N1\_S

USB20\_N1\_P

USB20\_P1\_S

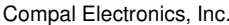
USB20\_P1\_P

DLW21HN600SQ2L\_4P

JUSBF CONN@

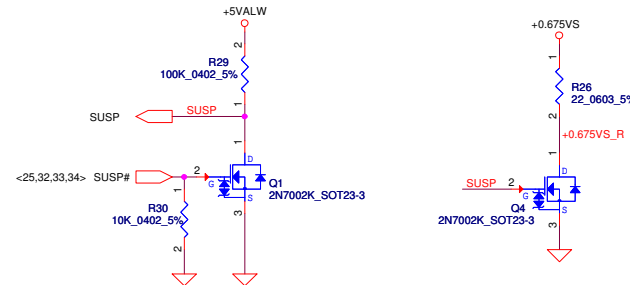
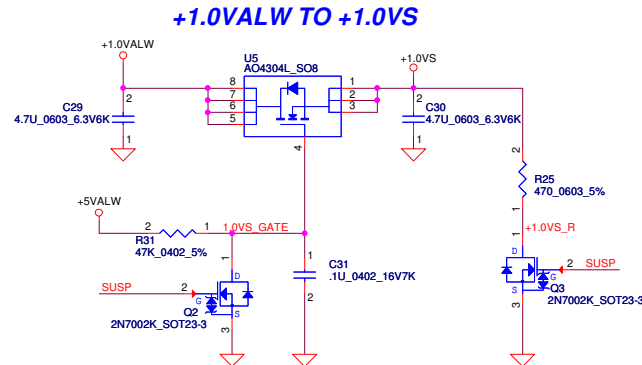
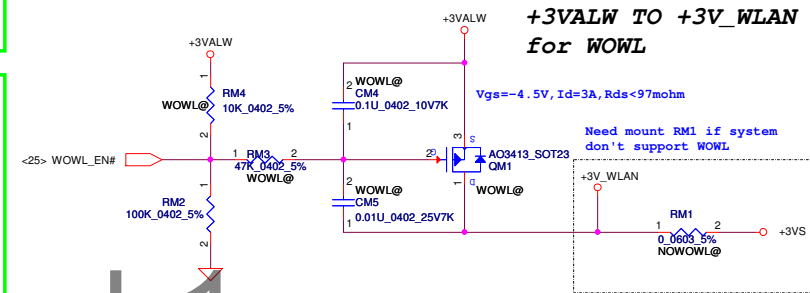
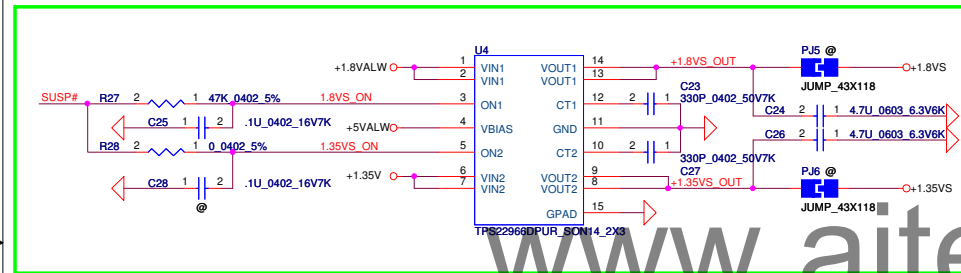
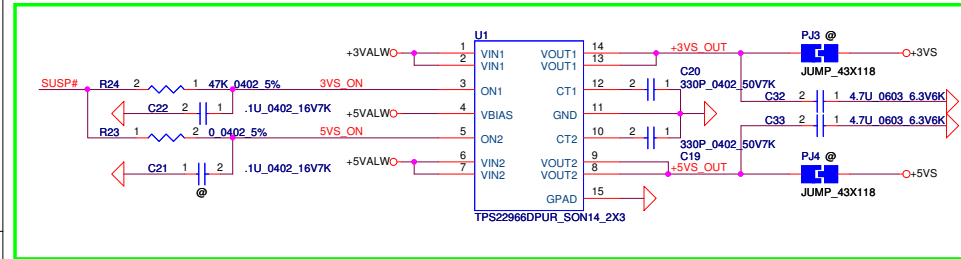
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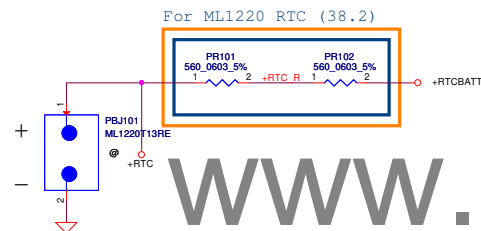
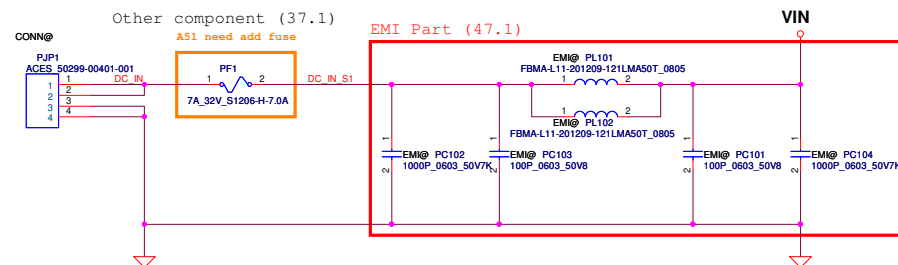




# Normall Platform (Not support M-STATE and Deep Sleep)



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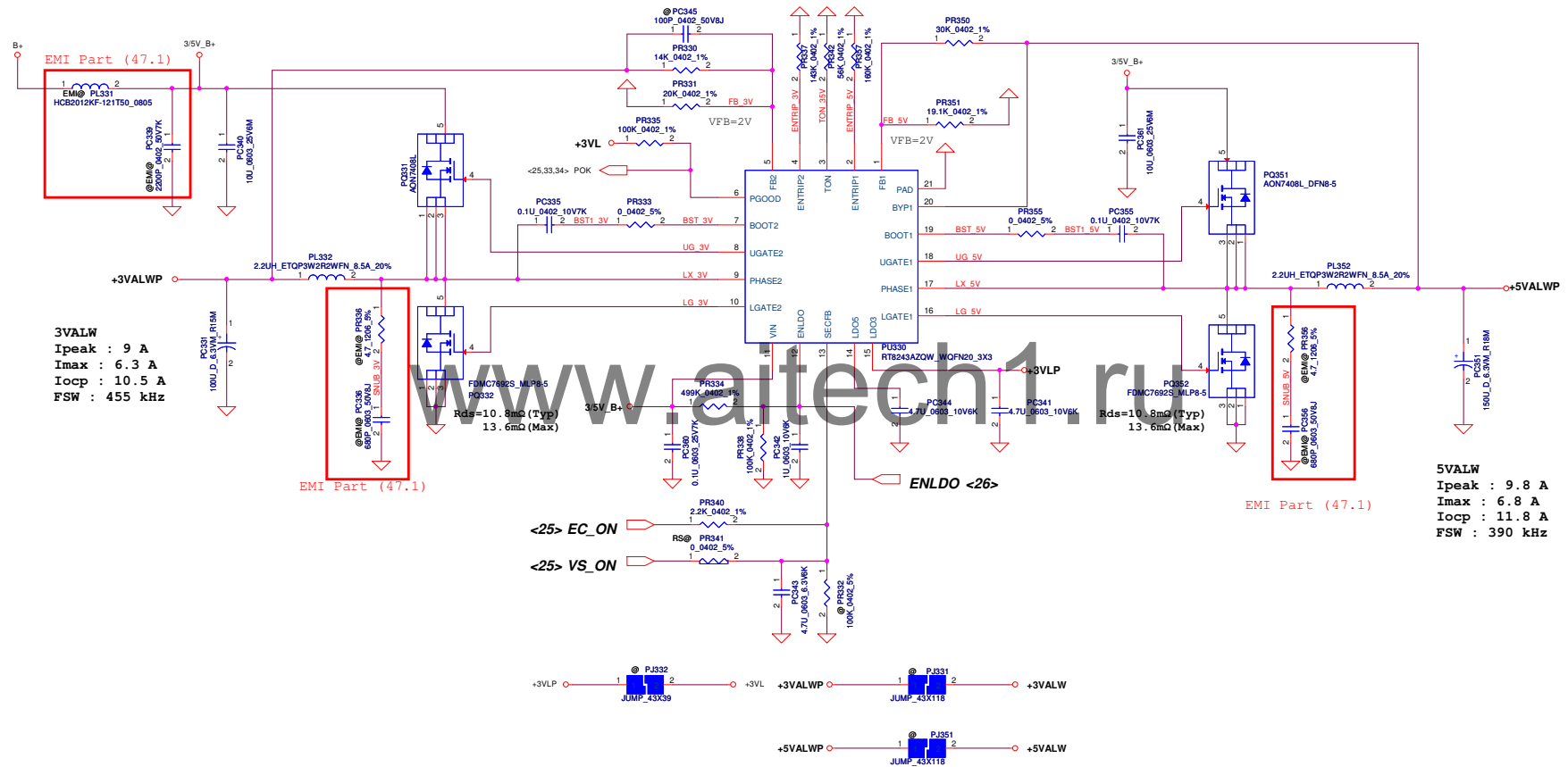


	Initial	Recovery
CPU OTP	90 C	70 C

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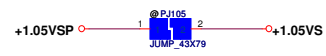
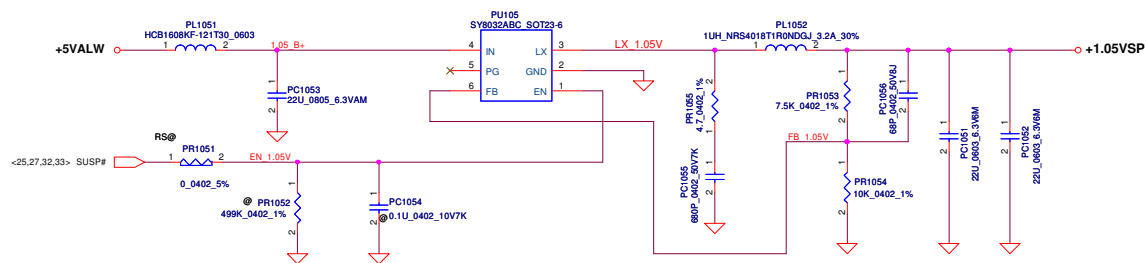
3/5VALW controller (35.1), Support component (35.2)



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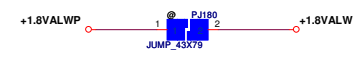
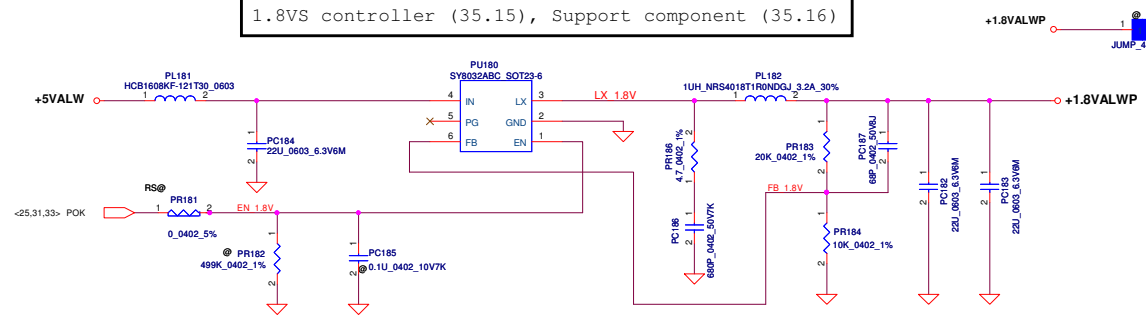




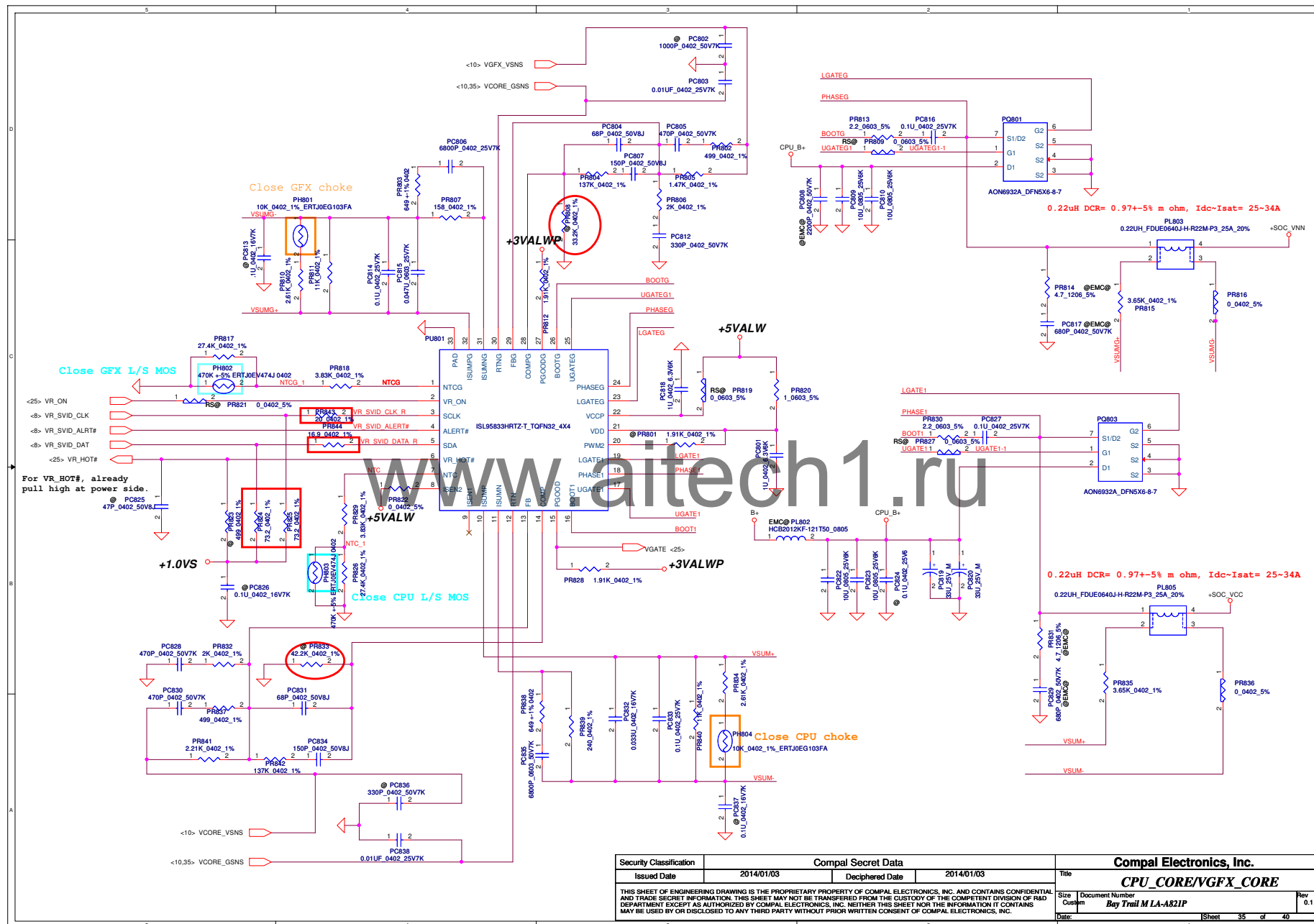


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1.8VS controller (35.15), Support component (35.16)



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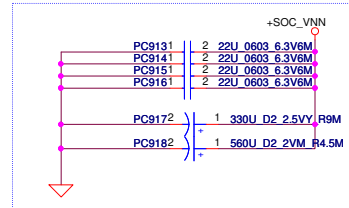
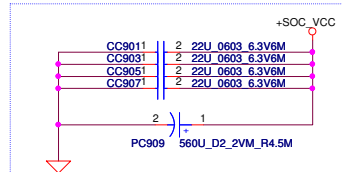


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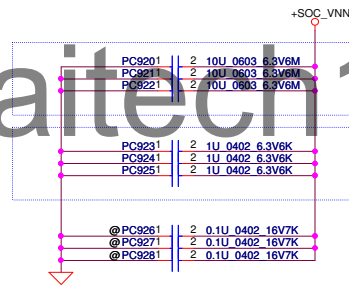
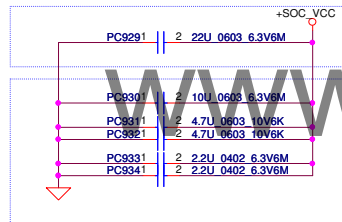
Output Cap

Package Edge Cap

Back Side Cap



Output Cap



Package Edge Cap

Back Side Cap

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Notes
POSCAP 330 $\mu$ F	2	6 m $\Omega$	1.8 nH	Output	1, 2
22 $\mu$ F 0805 X5R	4	3 m $\Omega$	0.6 nH	Output	

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Notes
POSCAP 330 $\mu$ F	3	6 m $\Omega$	1.8 nH	Output	1, 2
22 $\mu$ F 0805 X5R	4	3 m $\Omega$	0.6 nH	Output	

Package Pin Name	Back Side Cap	Package Edge Cap	Comments
CORE_VCC_S0IX	1X0603 10 $\mu$ F 2X0402 4.7 $\mu$ F 2X0402 2.2 $\mu$ F	3X0805 22 $\mu$ F	
UNCORE_VNN_S3	3X0402 1 $\mu$ F	3X0805 10 $\mu$ F	

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HW PIR (Product Improve Record)

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